IN THE SPECIFICATION:

Please replace paragraph number **[0002]** with the following rewritten paragraph:

[0002] State of the Art: Metal-Oxide-Semiconductor (MOS) is the primary technology for large-scale integrated semiconductor circuits. In Complementary MOS (CMOS) architectures, these semiconductor circuits combine two types of MOS devices, namely p-channel MOS (PMOS) devices and n-channel MOS (NMOS) devices, on the same integrated circuit. ~~A~~An MOS transistor is a four-terminal device which controls the current that flows between two of the terminals by activating and deactivating the voltage which is applied to the third or fourth terminal. FIG. 1 shows a cross-sectional diagram of a conventional n-channel MOS transistor 10. As shown in FIG. 1, transistor 10 includes spaced-apart n+ source and drain regions 12 and 14 which are formed in a p-type substrate 16, and a channel region 18 which is defined between source and drain regions 12 and 14. Source and drain regions 12 and 14, in turn, represent the first two terminals of the device while substrate 16 represents the third terminal.

Please replace paragraph number **[0003]** with the following rewritten paragraph:

[0003] Transistor 10 also includes a layer, illustrated as gate oxide 20, which is formed over channel region 18, and a gate 22 which is formed over gate oxide ~~layer~~ 20. Gate 22 represents the fourth terminal of the device. During operation of the transistor 10, electrons flow from source region 12 to drain region 14 when an electric field is established between source and drain regions 12 and 14. Furthermore, the drain-to-substrate junction is reverse biased when a gate voltage equal to or greater than the threshold voltage of transistor 10 is applied to gate 22. These conditions can be met, for example, when ground is applied to substrate 16 and source region 12, and one volt, for example, is applied to drain region 14.

Please replace paragraph number **[0004]** with the following rewritten paragraph:

[0004] A gate voltage applied to gate 22 attracts electrons to the surface adjacent to gate oxide 20 of substrate ~~10~~ 16 in channel region ~~16~~ 18. When a minimum number of electrons has been attracted to the surface of substrate 16 in channel region 18, the electrons form a channel which allows the electrons in source region 12 to flow to drain region 14 under the influence of the electric field. The threshold voltage is defined as the minimum gate voltage that must be applied to gate 22 to attract the minimum number of electrons to the surface of substrate 16 to form an electrically conductive inversion region in the channel region 18.

Please replace paragraph number **[0006]** with the following rewritten paragraph:

[0006] MOS transistors are formed using photolithographic processes according to design rules corresponding to a particular process. The design rules specify, among other things, the minimum length of the channel region. To gain performance advantages and as processing technology advancements have been achieved, the channel length between the source and drain has generally shortened. Furthermore, to minimize the silicon area consumed by ~~a~~ an MOS circuit, a typical integrated circuit design is largely implemented with transistors that have the minimum channel length. Since the circuit is largely implemented with transistors that have the minimum channel length, the fabrication process, for example the enhancement implant, is commonly optimized to adjust the threshold voltages of the transistors which have the minimum channel length. While performance improvement is generally a paramount objective for MOS circuit design, it is common for ~~circuits~~ circuits, in addition to utilizing transistors having minimum channel ~~length~~ length, to also require transistors which have channel lengths that are longer than the minimum. For those transistors with a longer channel length, a lower threshold voltage is realized when the threshold voltage is optimized for a shorter-channel transistor through the use of a single enhancement implant.

Please replace paragraph number **[0007]** with the following rewritten paragraph:

[0007] FIG. 2 is a graph that generally plots the threshold voltages as a function of channel length. As shown in FIG. 2, when the threshold voltage is optimized for an arbitrary ~~fabricatable~~ fabricable channel length x, the threshold voltage of a transistor decreases as the channel length of the transistor increases. Furthermore, the reduced threshold voltages of the longer channel devices lead to increased leakage currents which, in turn, are particularly undesirable in circuits which are utilized in battery-operated devices.

Please replace paragraph number **[0013]** with the following rewritten paragraph:

[0013] In yet a further embodiment of the present invention, a method for manufacturing a MOS structure on a semiconductor substrate is provided. A gate oxide layer is formed over the semiconductor substrate with a polysilicon layer also being ~~also~~ formed over the gate oxide layer. A first mask layer is formed and patterned followed by etching to form a gate. The gate includes an aperture between the source and drain ends of the polysilicon layer. Implant regions are formed in the substrate adjacent to the drain and source ends of the gate. Also, at least one implant region is formed in the substrate through the aperture of the gate. Source and drain regions are formed in the substrate adjacent to the source and drain ends of the gate.

Please replace paragraph number **[0023]** with the following rewritten paragraph:

[0023] While short channel transistors are susceptible to decreased threshold voltages and therefore utilize threshold voltage adjusting enhancement implants for adjusting the threshold voltage, short channel transistors are also susceptible to so-called "hot carrier effects." Generally, as the channel length is shortened, the maximum electric field E_m becomes more isolated near the drain side of the channel, causing a saturated condition that increases the maximum energy on the drain side of the MOS device. The high energy causes electrons in the channel region to become ~~"hot".~~ "hot." An electron generally becomes hot in the vicinity of the drain edge of the channel where the energy arises. Hot electrons can degrade device performance and cause breakdown of the device. Moreover, the hot electrons can overcome the potential

energy barrier between the silicon substrate and the silicon dioxide layer overlying the substrate, which causes hot electrons to be injected into the gate oxide.

Please replace paragraph number **[0027]** with the following rewritten paragraph:

[0027] In addition to the concern over hot carrier injection in short channels, a condition known as "punch-through" is also of concern. To further protect the transistor from punch-through conditions, a double diffusion (DD) process may further surround the LDDs. The DD process implants one or more dopants into the same region followed by a high temperature annealing step, in which the one or more dopants diffuse simultaneously, and form a structure called a double-diffused (DD) region, also commonly called a double-diffused drain (DDD). In an exemplary DD process, a medium phosphorus dose and a heavy arsenic dose may be implanted; but in both ~~case~~ cases a p-type Boron halo implant is put in to surround the n-type LDD implant to protect against "punch-through." The faster-diffusing phosphorus is driven farther under the gate edge than the arsenic, creating a less abrupt concentration gradient for the drain.

Please replace paragraph number **[0028]** with the following rewritten paragraph:

[0028] When transistor channel lengths are several times longer than the diameter of the LDD and DD regions, ~~then~~ the threshold voltage adjusting or enhancement implant exhibits the ~~dominate~~ dominant effect over the other adjacent implants. However, as fabrication processes improve, transistor channel lengths generally decrease. In short-channel transistors that include one or both of an LDD or DD region, the LDD or DD implant ~~diffusions~~ diffusions, with their larger dopant ~~concentrations~~ concentrations, more greatly influence the threshold voltage adjustment than does the enhancement implant. Therefore, processes that include both short and long channels would necessarily exhibit differing threshold voltages since the threshold voltage of short-channel transistors is more greatly influenced by the LDD and DD implants while the threshold voltage of the long-channel transistors is more greatly influenced by the threshold voltage adjusting enhancement implant.

Please replace paragraph number **[0029]** with the following rewritten paragraph:

[0029] FIG. 3 is a perspective view of a transistor incorporating a channel implant process, in accordance with an embodiment of the present invention. A transistor 30 is formed upon and within a substrate 42 and generally includes a gate 32 formed upon a gate oxide 28 according to processes known by those of ordinary skill in the art. Transistor 30 further includes a drain region 48 and a respective source region 50 generally formed within substrate 42. In accordance with the channel implant process of an embodiment of the present invention, gate 32 further includes one or more apertures 34, 36 formed within the general body of gate 32. Apertures 34, 36 provide internal implant windows 38, 40 into the channel region 52 located generally below gate 32. The quantity of apertures 34, 36 is a function of the dimensions of the channel, namely channel length 44 and channel width 46. As viewed in a top view, apertures 34, 36 may be in the shape of a square, rectangle, circle, polygon, or any other uniform or non-uniform shape. However, a square aperture is shown in the drawing figures, and used as an example hereinafter. Additionally, the aperture, when viewed from the top, may be entirely or partially enclosed or surrounded by gate 32. For example, the aperture may be located on the edge of the gate 32 and not entirely enclosed with the gate material resulting in a notch, ~~grove,~~ groove, keyhole, or the like. However, it is currently preferred that the aperture be enclosed within gate 32. The aperture may be formed by conventional mask and etch procedures either before or after the ~~gate~~ aperture 34 is formed.

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] In most typical LDD structures for CMOS devices, sources/drains are formed by four implants with dopants, each implant requiring a masking step. The four masking steps are: a first mask (a P-LDD mask) to form the P-LDD structures, a second mask (an N-LDD mask) to form the N-LDD structures, a third mask (a P+ S/D mask) to form the p-type doped, deep source/drain junctions, and a fourth mask (an N+ S/D mask) to form the N-type doped, deep source/drain junctions. Each masking step typically includes the sequential steps of preparing the

semiconductor substrate, applying a photoresist material, soft-baking, patterning and etching the photoresist to form the respective mask, hard-baking, implanting a desired dose of a dopant with the required conductivity type, stripping the photoresist, and then cleaning of the ~~substrate~~ substrate 24.

Please replace paragraph number **[0037]** with the following rewritten paragraph:

[0037] FIG. 5B illustrates the process for forming an LDD structure, in accordance with an embodiment of the present invention. In this process, a gate insulating oxide 90 is formed over the previously defined channel region 52 with a gate layer 92, such as a polysilicon layer, deposited over gate insulating oxide ~~layer~~ 90. Furthermore, gate 32 has formed therein one or more apertures 34, 36 for facilitating implantation within the outer periphery of gate 32. Using gate 32 as a mask, impurity ions, for example n-type impurity ~~ions~~ ions, are generally vertically implanted as LDD implant 94 into substrate 42 in a low concentration, thereby forming LDD structures 96, 98, 100, 102.

Please replace paragraph number **[0039]** with the following rewritten paragraph:

[0039] In an annealing process as depicted in FIG. 5D, the various implantation ions of both the LDD implants 94 and DD implants 104 result in further penetration of the implant ions into substrate 42. As illustrated, the LDD ~~or n- regions~~ structures (or n- regions) 96-102 as well as the DD implant regions 106-112 migrate under the channel region 52 located under the gate 32. Migration of the higher dopant concentrations of the LDD implants and the DD implants minimizes the impact of the enhancement implant of FIG. 5A and causes the threshold voltage to change according to the additional dopant concentrations.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

[0040] In FIG. 5E, spacers 114, 116 as well as implant shields 118, 120 protect the underlying structures from the high concentration source/drain implant 122 while the source region 50 and drain region 48 are implanted. As illustrated in FIG. 5F, spacers 114, 116 and

implant shields 118, 120 are removed to complete the formation of transistor 30. As illustrated, transistor 30 is comprised of a gate 32, drain and source regions 48, 50 as well as drain and source specific LDD structures 54, 56 and drain and source specific DD structures 62, 64. Transistor 30 further comprises one or more internal LDD structures 58, 60 as well as one or more internal DD structures ~~or regions~~ (or regions) 68, 70. The formation of internal ~~structures~~ structures, through the use of implants throughout the length of the ~~channel~~ channel, more consistently aligns the threshold voltage of a long channel transistor with the threshold voltage of a short channel transistor and thereby reduces the disparate threshold voltages between respective long and short channel transistors while eliminating independent threshold voltage enhancement implants for long and short channel transistors.

Please replace paragraph number **[0041]** with the following rewritten paragraph:

[0041] FIGS. 6 and 7 illustrate grid arrangements of apertures, according to specific embodiments of the present invention. In FIG. 6, the formation of a gate 32 includes an exemplary pattern of apertures 136 for the gate 134 shown in a "checkerboard" pattern between a source region 138 and a drain region 140. In addition, an exemplary method for calculating the width of aperture 136 with respect to gate 134 height and implantation angle (b) is shown in FIG. 8. One current exemplary embodiment includes a gate length of about ~~.1~~ 0.1 to 4 microns. FIG. 7 illustrates the formation of apertures in a gate, in accordance with another embodiment of the present invention. A gate 142 includes an exemplary two-dimensional array of apertures 144 located between a source region 146 and a drain region 148. Further geometries and aperture shapes are also contemplated within the scope of the present invention.

Please replace paragraph number **[0042]** with the following rewritten paragraph:

[0042] FIG. 8 illustrates an exemplary ~~aperture,~~ aperture in accordance with an embodiment of the present invention. The dimensions (A) 150 of an aperture 152 may be determined by the gate height, desired ion implantation angle (b) 154, and process or manufacturing capabilities. For example, as shown in FIG. 8, if the gate height is 1200 Å and the

desired implantation angle (b) is 65°, the ~~aperture width~~ dimension (A) 150 would be (1200Å / tan 65°) or 560 Å. With current process or manufacturing capabilities, the aperture 152 dimensions are currently preferred to be greater than ~~.02~~ 0.02 by ~~.02~~ 0.02 microns. However, the aperture 152 dimension (A) should be small enough to allow the fringe effects from the gate field to electrically invert the charge of the area under the aperture when a voltage is applied to the gate.